42. (New) The insulated gate semiconductor device according to claim 40, further comprising a sixth semiconductor layer of said second conductivity type higher in an impurity concentration than said second semiconductor layer provided between said first and second semiconductor layers.

fig. 3
Cont
F2
fig. 22

43. (New) The insulated gate semiconductor device according to claim 42, wherein said sixth semiconductor layer extends through said first semiconductor layer and is partially exposed in said second main surface of said first semiconductor layer.

44. (New) The insulated gate semiconductor device according to claim 40, wherein said first main electrode is not contacting any other semiconductor layer than said fourth and fifth semiconductor layers.

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REMARKS

Favorable reconsideration of this application, in view of the following comments and as presently amended, is respectfully requested.

It is first noted that the outstanding Office Action has improperly been made a final rejection. More specifically, in the previous Office Action Applicants submitted a response to place the application in condition for allowance based on the previous indication of the allowable subject matter. The outstanding Office Action has now taken a new position and indicated that the previous response did not place the application in condition for allowance as two new grounds for rejection are set forth in the Office Action.

It is improper to set forth such new grounds for rejection in a final rejection. That is, Applicants are clearly entitled an opportunity to amend the claims in response to the outstanding new rejections set forth in the outstanding Office Action, and therefore the finality of the outstanding Office Action is improper.

In such ways, the present response must be entered.

Claims 22-26 and 40-44 are pending in this application. Claim 22 is amended and new Claims 40-44 are added by the present response. Claims 22-26 were rejected under 35 U.S.C. § 112, first paragraph. Claims 22, 24, and 26 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,644,148 to Kinzer. Claims 23 and 25 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kinzer.

Addressing now the rejection of Claims 22-26 under 35 U.S.C. § 112, first paragraph, that rejection is traversed by the present response.

The outstanding Office Action rejected Claims 22-26 as not clearly setting forth the channel regions. In response to that rejection it is noted that Claim 22 is amended by the present response to clearly indicate that "channel regions" are formed at each spot at which the insulating film is provided on portions of the fourth semiconductor layer interposed between the third and fifth semiconductor layers. Such channel regions are shown as elements 53, as non-limiting examples, in the drawings. It is respectfully submitted that the specification makes it clear that it is only those regions 53 that form channel regions.

Moreover, it is clearly recited in the present specification at page 22, lines 6-21, and with respect to the discussion of Figure 3, that a portion denoted by reference numeral 53 is a channel region. It is also clear from the configuration shown in Figure 3 that no channel region is formed at a portion other than the portion of the reference numeral 53, and a plurality of portions denoted by the reference numeral 53 is the only channel region in the insulated gate type semiconductor device.

The presently submitted amendment to Claim and the above comments are believed to address the rejection of Claims 22-26 under 35 U.S.C. § 112, first paragraph.

Addressing now the rejection of Claims 22, 24, and 26 under 35 U.S.C. § 102(e) as

anticipated by Kinzer, and the rejection of Claims 23 and 25 under 35 U.S.C. § 103(a) as unpatentable over Kinzer, those rejections are traversed by the present response.

Kinzer differs from the claimed invention in that Kinzer does not disclose or suggest the specific features of the "insulating film" and "control electrode" recited in independent Claim 22, and the claims dependent therefrom.

According to Claim 22, an "insulating film [is] provided on portions of said fourth semiconductor layer interposed between said third and fifth semiconductor layers" and "a control electrode [faces] said portions through said insulating films so that said portions form channel regions as only channel regions of said insulated gate semiconductor device". Such features clearly distinguish over the teachings in Kinzer.

The outstanding Office Action cites element 95 in Kinzer as corresponding to the claimed "insulating film" and element 114 as corresponding to the claimed "control electrode". However, it is respectfully submitted that it is clear that element 95 in Kinzer, labeled only in Figure 14 of Kinzer, is not provided on portions of the fourth semiconductor layer 81 in Kinzer interposed between the third semiconductor layer 61 and the fifth semiconductor layer 131, as those other layers are relied upon in the teachings in Kinzer.

Further, the electrode 114 in Kinzer does not face portions at which an insulating film is provided on a fourth semiconductor layer, i.e., in Kinzer the electrode 114 does not face portions on which the insulating film 95 is provided on portions of the fourth semiconductor layer 81, so that those portions form the only channel regions of the insulated gate semiconductor device.

In such ways, the invention as recited in independent Claim 22, and the claims dependent therefrom, patentably distinguishes over the teachings in Kinzer.

The present response also sets forth new Claims 40-44 for examination. New

independent Claim 40 is similar to amended independent Claim 22 except that new independent Claim 40 even further defines that the third semiconductor layer directly contacts with the second semiconductor layer and such "that the fourth semiconductor layer does not contact with said semiconductor layer". According to that feature recited in new independent Claim 40, and with reference to Figure 3 in the present specification as a non-limiting example, the third semiconductor layer 43 is interposed between the second semiconductor layer 42 and the fourth semiconductor layer 44 such that the fourth semiconductor layer 44 does not contact with the second semiconductor layer 42. That feature clearly distinguishes over the outstanding rejection relying upon the teachings in Kinzer as in Kinzer the relied upon fourth semiconductor layer 81 clearly contacts the relied upon second semiconductor layer 52, as shown in Figure 19 of Kinzer. Thus, new independent Claim 40, and the claims dependent therefrom, even further define over the teachings in Kinzer.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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IN THE CLAIMS

22. (Four Times Amended) An insulated gate semiconductor device, comprising:

a first semiconductor layer of a first conductivity type having first and second main surfaces on opposite sides thereof;

a second semiconductor layer of a second conductivity type provided on said first main surface of said first semiconductor layer;

a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer, wherein said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer and is in direct contact with said second semiconductor layer;

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on [a portion] portions of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said [portion] portions through said insulating film so that said [portion forms] portions form [a] channel [region] regions as [an] only channel [region] regions of said insulated gate semiconductor device.

40-44. (New).